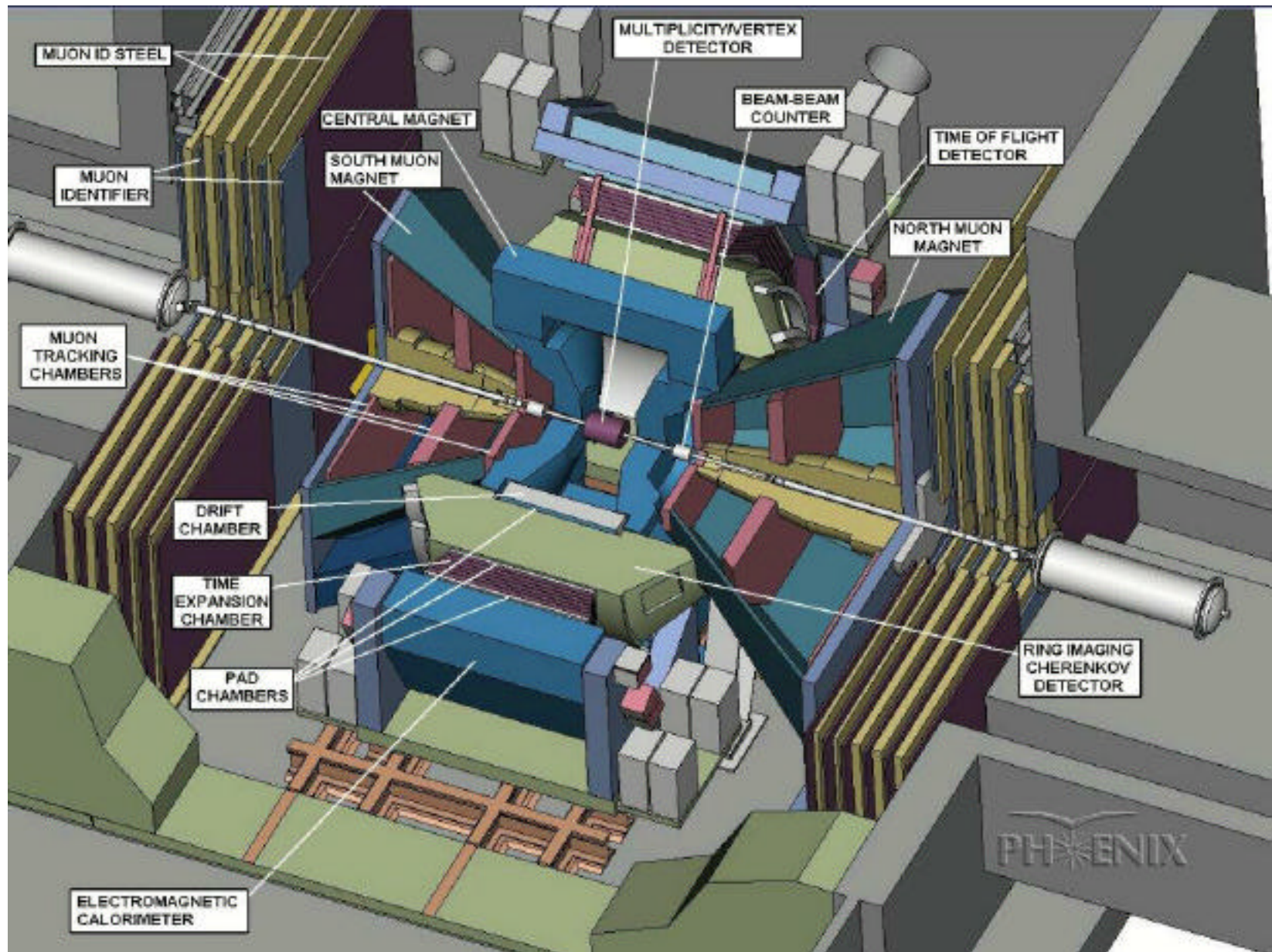


# The PHENIX Multiplicity and Vertex Detector

**Michael Bennett**  
**Los Alamos National Laboratory**  
**for the PHENIX MVD group**

1. Overview
2. Design Challenges
3. Performance
4. Status



## MVD Overview:

### Physics goals:

Charged particle multiplicity

Centrality trigger at LVL-1

Collision vertex position

**simulated 3-d vertex to  $200\mu\text{m}$**

$dN/d$        $d^2N/d^2$

### Design Challenges:

Large acceptance (  $\eta = 5$ , full )

High granularity (large track density)

Minimal material in electron arm acceptance

Compact Read-out electronics

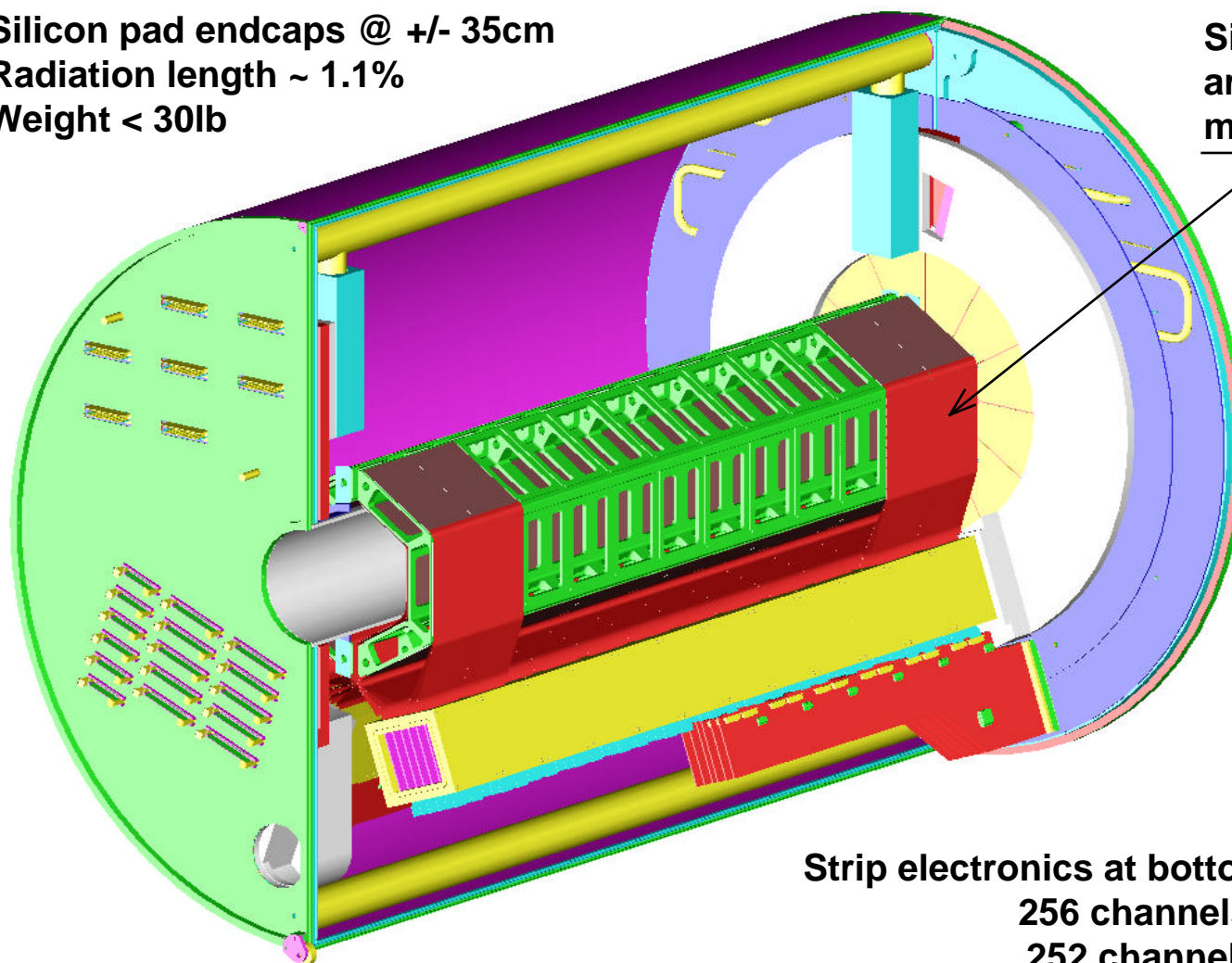
**Clamshell design - mounts to magnet pole faces.**

**Inner and outer barrels of silicon strip detectors, 200 $\mu$ m, 64cm length**

**Silicon pad endcaps @ +/- 35cm**

**Radiation length ~ 1.1%**

**Weight < 30lb**

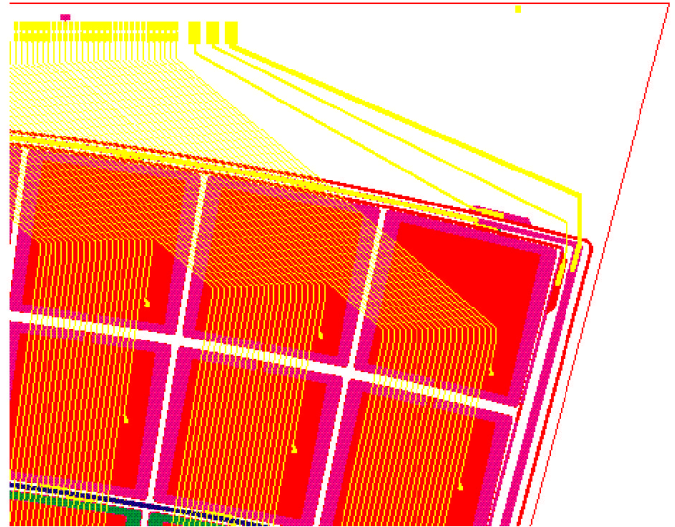
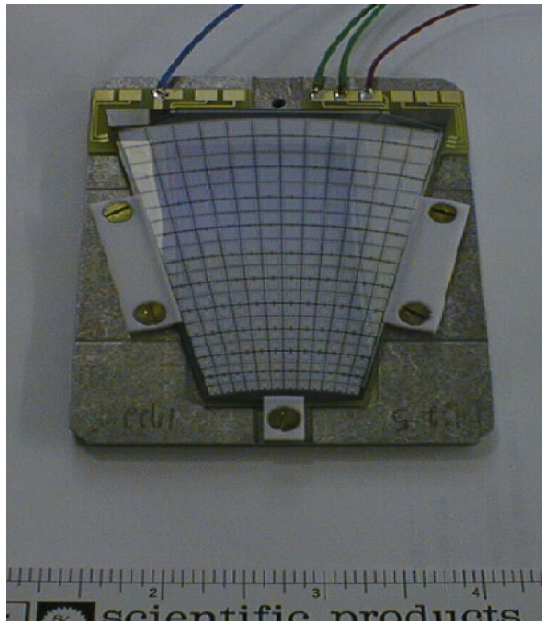


**Silicon strip detectors  
are mounted in sections  
marked red.**

**Strip electronics at bottom - Multi-Chip Module**  
**256 channels/silicon strip detector**  
**252 channels/silicon pad detector**  
**Total channel count = 34,720**

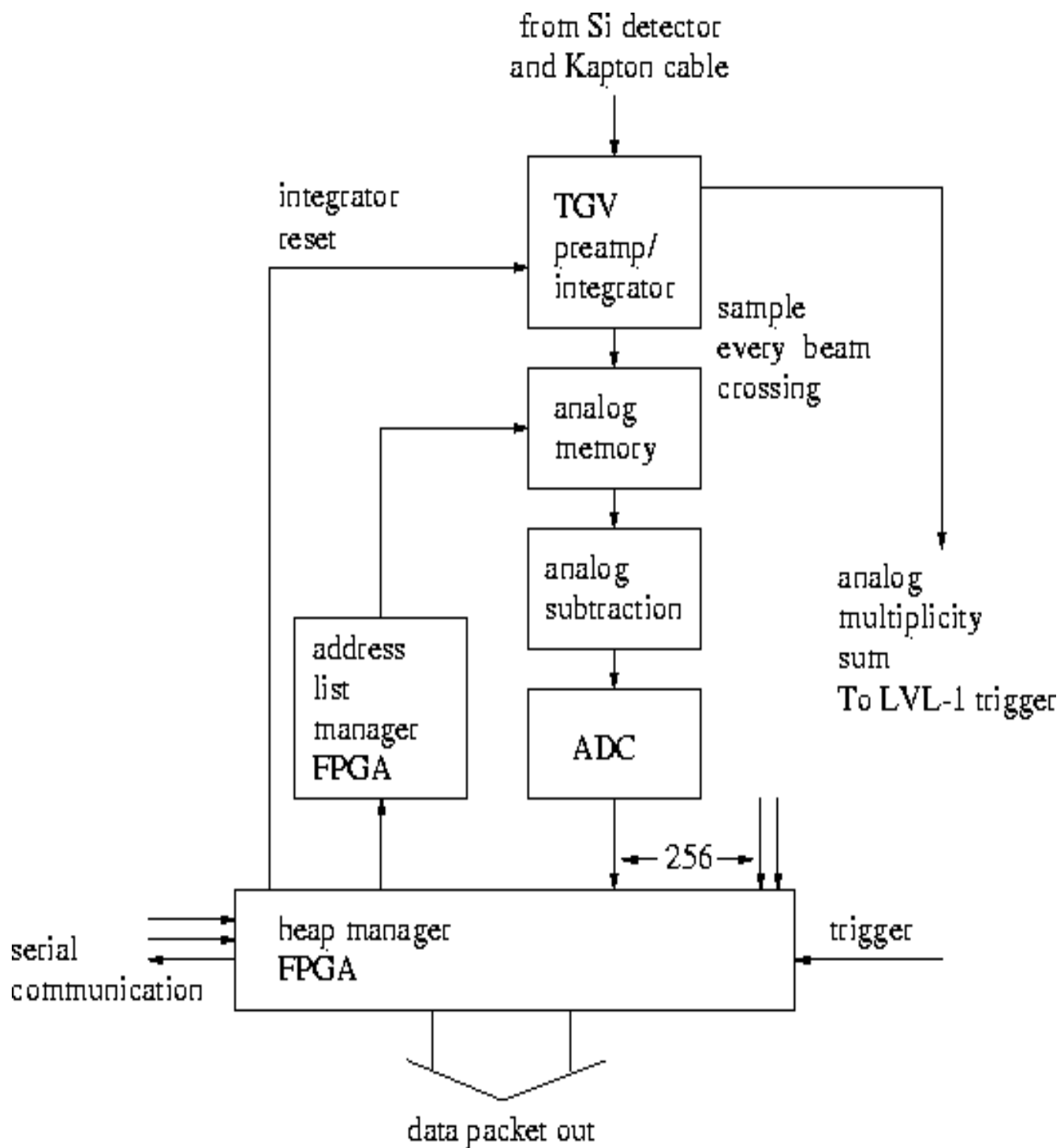


## Double Metal Pad Detector

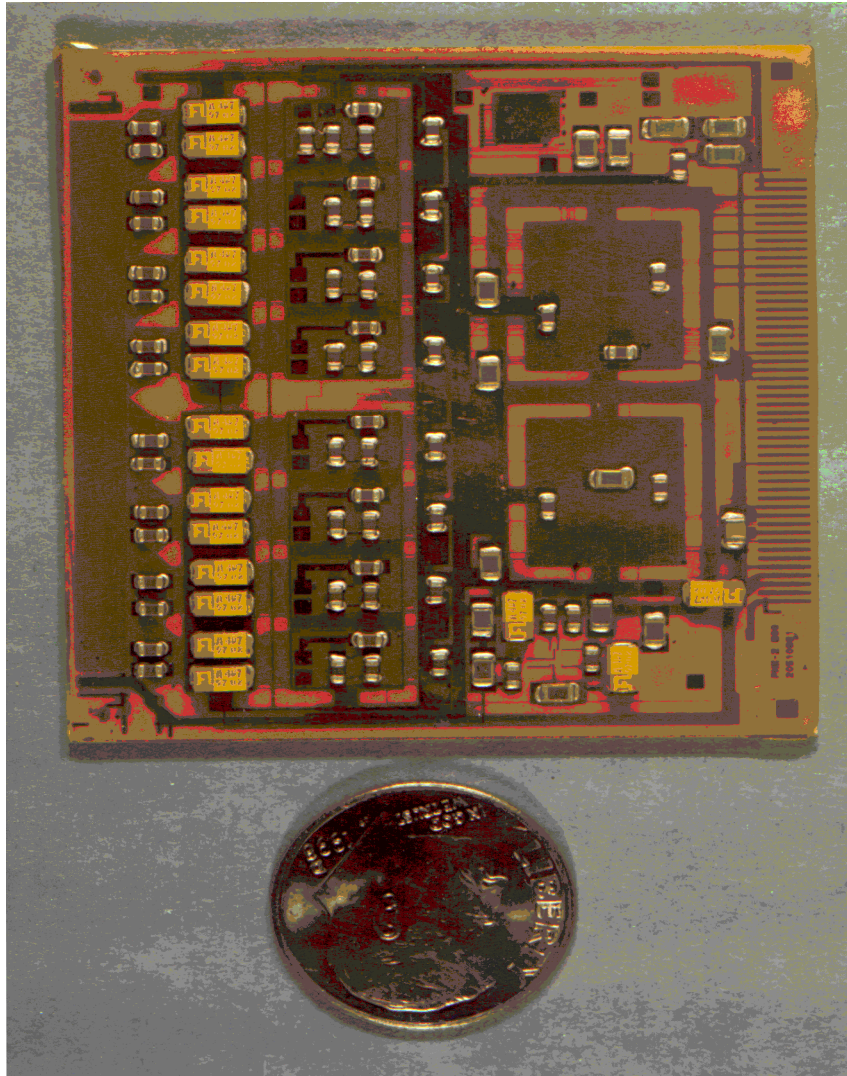


- Eliminates specialized kapton cable
- Reduces wirebonding
- Facilitates detector probe tests
- Facilitates assembly and handling

## MVD front-end electronics Multi-Chip Module



## Mechanical Sample of MCM with Surface Mount Components



**136 MCM's**  
**34,720 channels**

## $dN/d\eta$ in the MVD

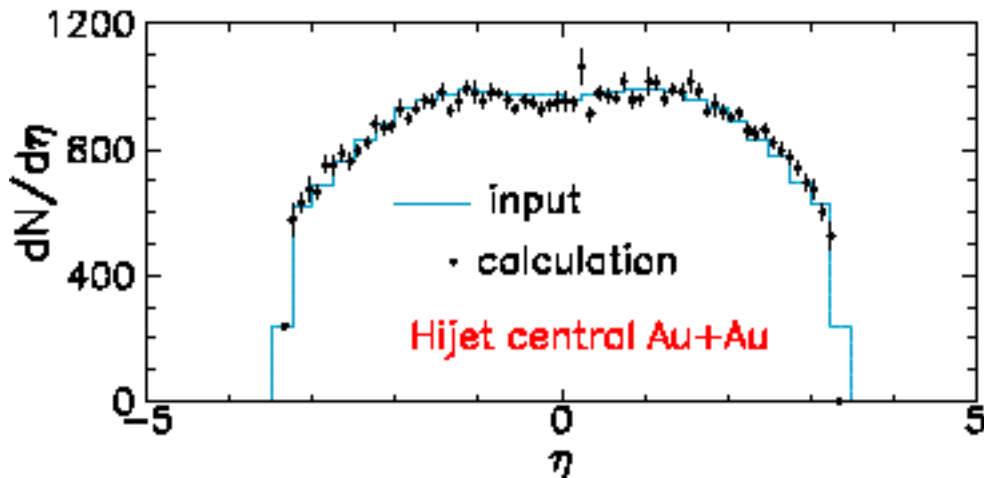
### Strip Detectors:

Gain-corrected ADC values are adjusted for path length in Si, summed over some chosen grouping of strips, then divided by average MIP energy deposition to get number of hits. Can be binned in  $\eta$ .

### Pad Detectors:

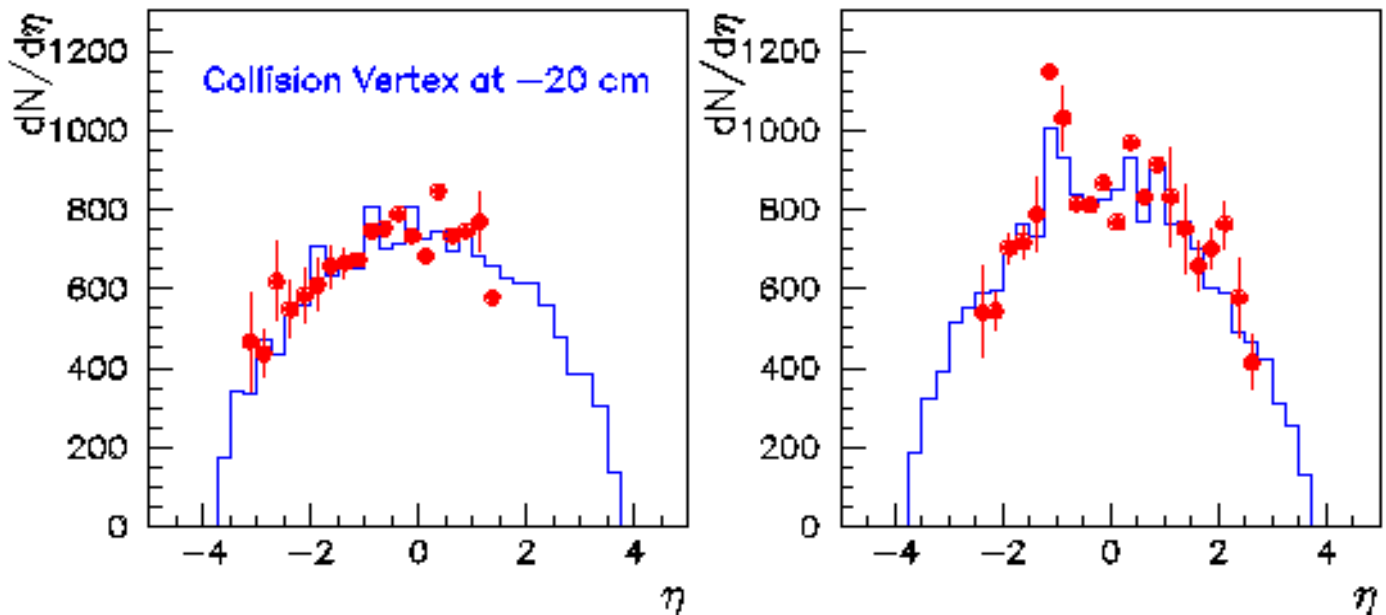
Gain-Corrected ADC values are adjusted for path length in Si, then normalized to expected MIP value. Number of hits for this pad are assigned based on Poisson statistics and overall occupancy. Each pad covers  $\Delta\eta = 0.04$  and  $\sim 2.5^\circ$  in  $\phi$ .

## Average $dN/d\eta$ , 125 HIJET events

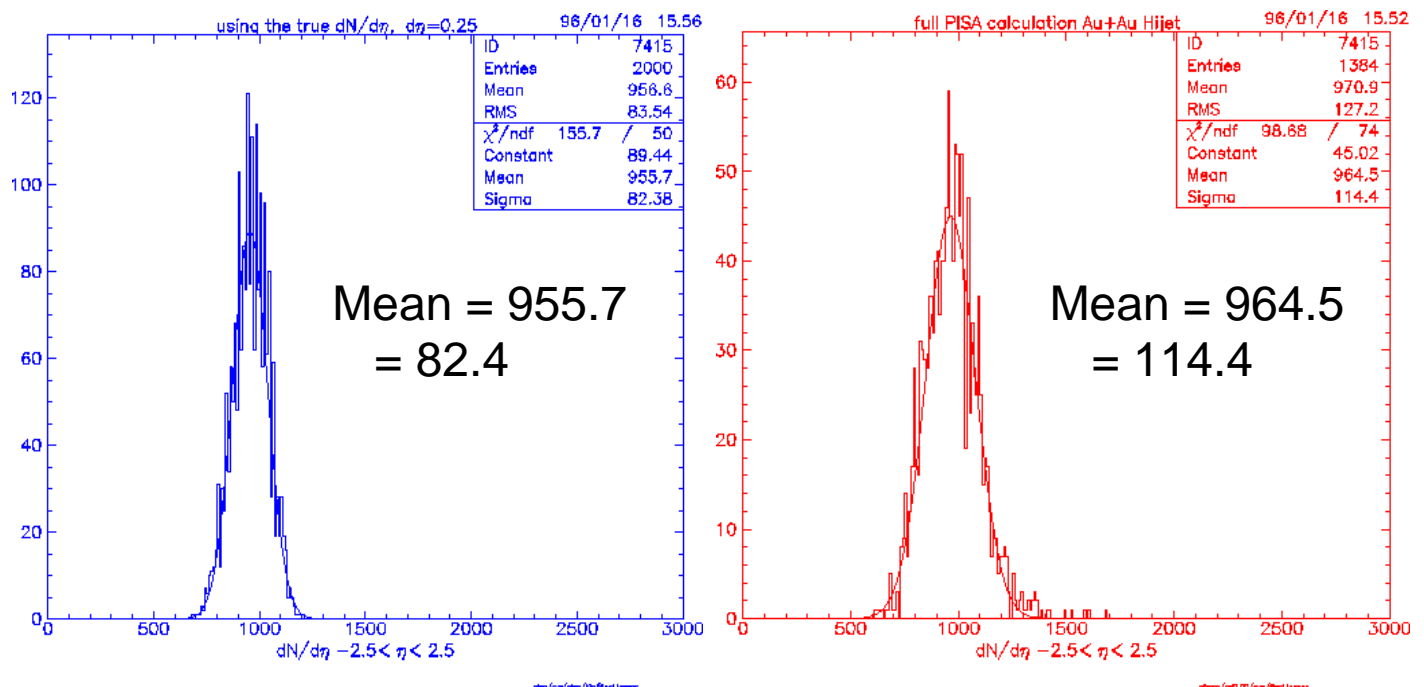




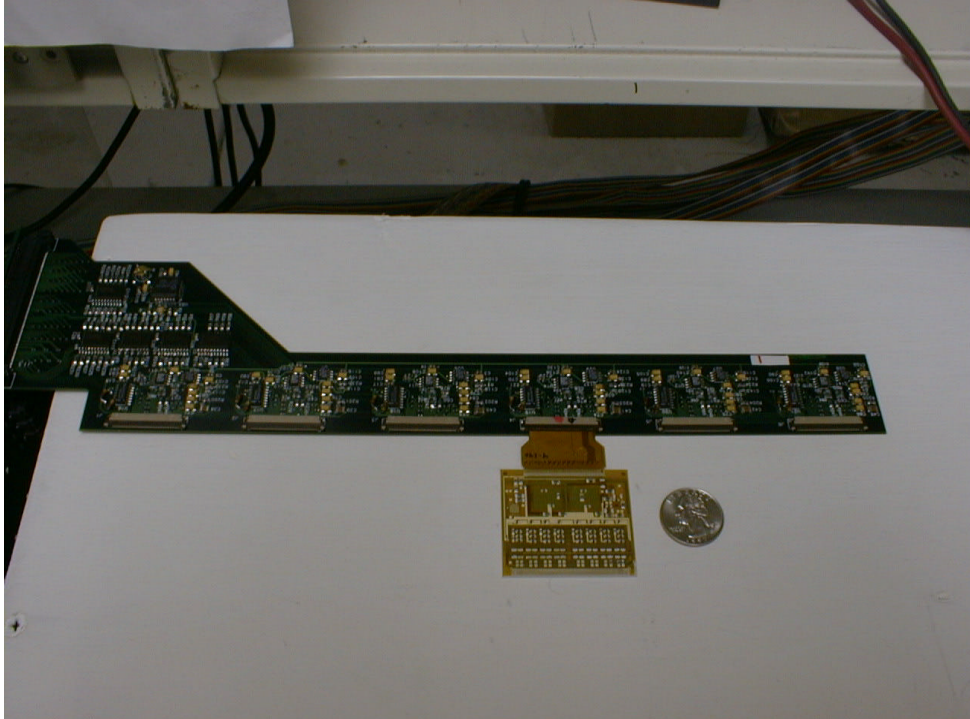
# $dN/d\eta$ for Single HIJING Events



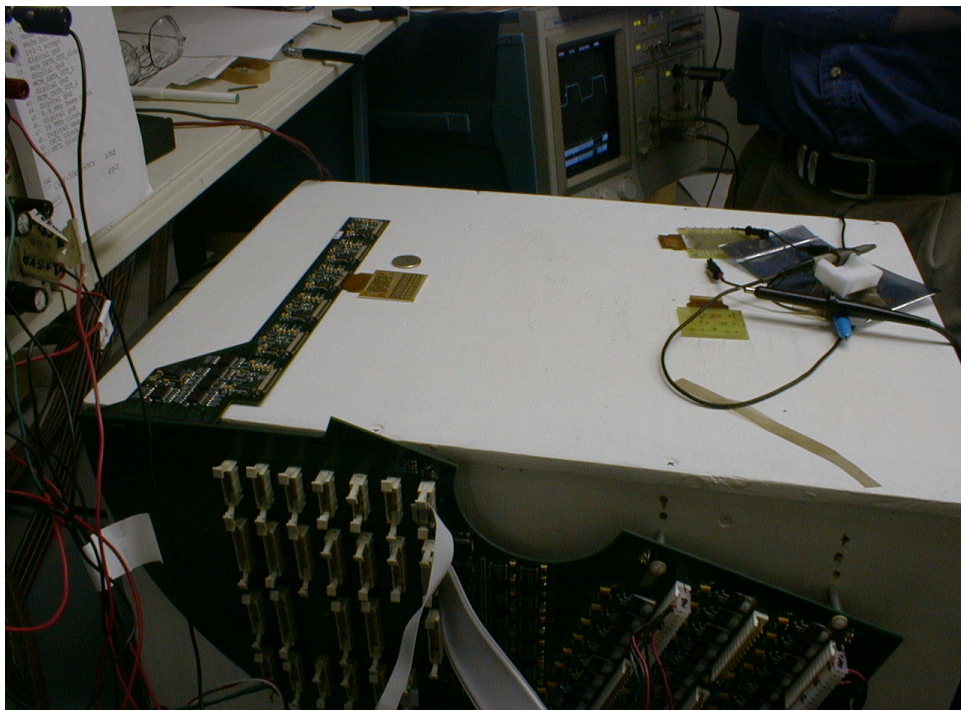
## Spread in intrinsic and MVD $dN/d\eta$ (HIJET events -2.5                      2.5)



## MCM Testing Underway

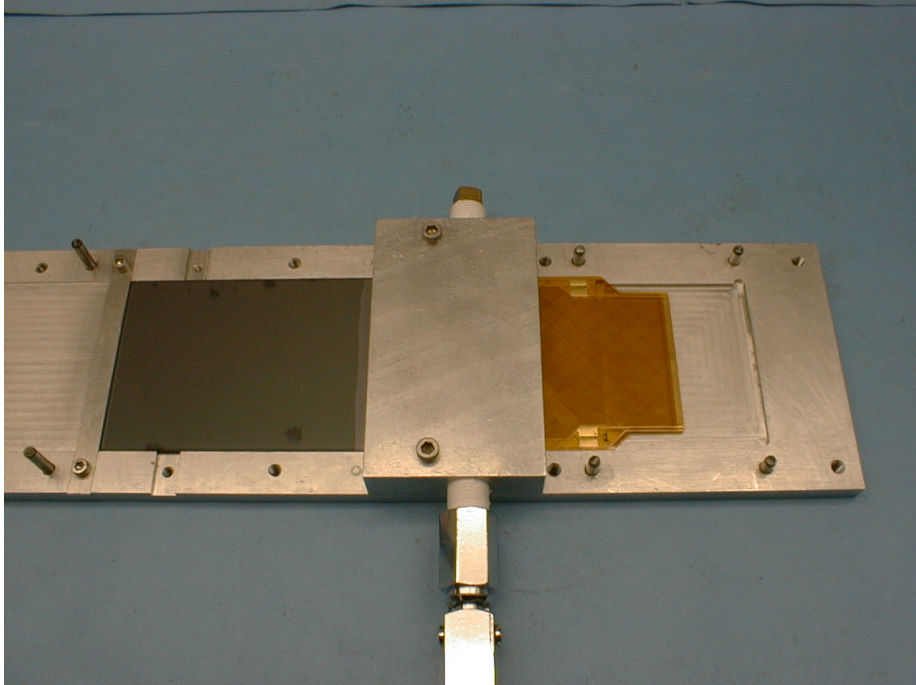


**MCM +  
Power-Comm  
Board**

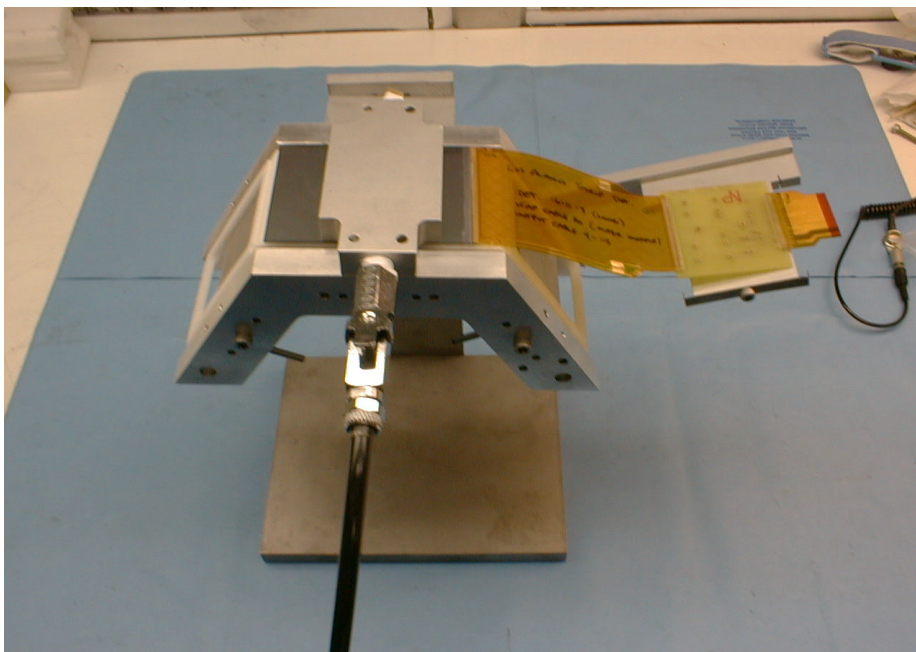


**MCM +  
Power-Comm  
Board +  
Mother Board**

## Mechanical Construction in Progress



Gluingsi - kapton cable  
- MCM  
assemblies



Developing  
procedure  
for gluing  
assemblies to  
Rohacell  
C-Cages



# MVD Construction Status



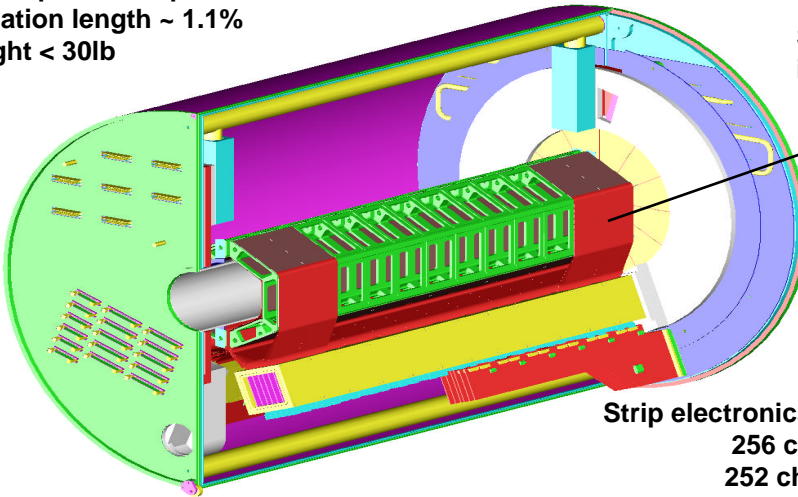
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Silicon strip detectors are mounted in sections marked **red**.

Strip electronics at bottom - Multi-Chip Module  
256 channels/silicon strip detector  
252 channels/silicon pad detector  
Total channel count = 34,720

**All mechanical and electronic components are prototyped or in fabrication**

**Si pad detectors are in production**

**final batch currently in testing**

**Si microstrip detectors are in production**

**full complement in hand, now testing spares**

**Rohacell C-cages have been produced at UCR.**

**All custom chips are manufactured.**

**First production MCM's are in hand**

**testing with associated boards underway**

**All custom electronics boards are in fabrication.**

**All kapton cables are in production**

**Si / cable assemblies being glued and wirebonded**

**Cooling system is currently being assembled.**

**Construction expected to complete at LANL in fall 1999.**





## **PHENIX MVD Group**

**Project Leader & Detector Council Member:** J. Simon-Gillo (LANL)  
**Mechanical Coordinating Physicist:** J. Simon-Gillo (LANL)  
**Electronics Coordinating Physicist:** J.P. Sullivan (LANL)  
**Lead Mechanical Engineer:** J. Boissevain (LANL)  
**Lead Silicon Design and Electronics Engineer:** S. Hahn (LANL)  
**Lead Integrated Chip Design Engineer:** C.L. Britton (ORNL)  
**Lead Interface Module Engineer:** N. Ericson (ORNL)  
**Systems Integration Engineer:** J. Boissevain (LANL)  
**Lead MCM Engineer:** G. Smith (LANL)  
**Lead MCM Designer:** Gary Richardson (LANL)  
**Simulation Computing:** M.J. Bennett (LANL)  
**Off-line Computing:** J.P. Sullivan (LANL)  
**On-line Computing:** H. van Hecke (LANL)  
**Database Coordinator:** M.J. Bennett (LANL)  
**Construction Manager:** M.J. Bennett (LANL)  
**Silicon Production and Testing Coordinator:** D. Jaffe (LANL)

**Institutions:** Los Alamos National Laboratory  
Oak Ridge National Laboratory  
University of California at Riverside  
Yonsei University  
University of Alabama in Huntsville.

**5 Institutions**

**38 Participants**